

REMARKS

Applicant respectfully requests reconsideration of the present application in view of the foregoing amendments and in view of the reasons that follow.

Status of Claims:

No claims are currently being cancelled or added.

Claims 1, 2, 5-9, 13, 16, 20 and 21 are currently being amended.

This amendment and reply amends claims in this application. A detailed listing of all claims that are, or were, in the application, irrespective of whether the claims remain under examination in the application, is presented, with an appropriate defined status identifier.

After amending the claims as set forth above, 1-21 remain pending in this application.

Claim Rejections – 35 U.S.C. § 101:

In the Office Action, claims 1-21 were rejected under 35 U.S.C. § 101 as being to non-statutory subject matter, for the reasons set forth on pages 2, 4 and 5 of the Office Action. Please note that the claims recite “useful, concrete and tangible” results. For example, independent claim 1 recites means for determining, based on the logic cones, whether logic circuits that have been designed in a behavioral synthesis phase are acceptable to be used in a manufacturing phase for the logic circuits. Clearly, these claim features correspond to a useful, concrete and tangible result, in that, based on the logic cones, it is determines whether logic circuits that have been designed in a behavioral synthesis phase are acceptable to be used in a manufacturing phase. If the Examiner is to maintain this rejection, he is respectfully requested to explain how this does not correspond to a useful, concrete and tangible result. The other independent claims recite similar features at the ends of those claims.

Accordingly, all of the presently pending claims are believed to fully comply with 35 U.S.C. § 101.

Claim Rejections – 35 U.S.C. § 112, 2nd Paragraph:

In the Office Action, claims 1-21 were rejected under 35 U.S.C. § 112, 2nd Paragraph, as being indefinite, for the reasons set forth on pages 5 and 6 of the Office Action. This rejection is respectfully traversed. In particular, by extracting logic cones from machine-executable object code compiled from a behavioral level description written in a

programming language, a determining means determines whether logic circuits that have been designed in a behavioral synthesis phase are acceptable to be used in a manufacturing phase for the logic circuits.. The specification provides a clear description of the present invention, and one skilled in the art would readily understand how to use the present invention based on that description. Note that dependent claim 2 recites that first logic cones are compared to second logic cones to determine acceptability of logic circuits that have been designed in a behavioral synthesis phase. This is one way that the determination can be made. The Examiner's comments on page 6 of the Office Action concerning missing features from the claims is incorrect, since a means plus function claim element brings in features from the specification that describe the claimed function.

Accordingly, all of the presently pending claims are fully compliant with 35 U.S.C. § 112, 2nd Paragraph.

Claim Rejections – Prior Art:

In the Office Action, claims 1-21 were rejected under 35 U.S.C. § 102(e) as being anticipated by “Applied Boolean Equivalence Verification and RTL Static Sign-Off”, by Harry Foster; claims 1-21 were rejected under 35 U.S.C. § 102(b) as being anticipated by “As good as gold”, by Blackett; and claims 1-21 were rejected under 35 U.S.C. § 102(b) as being anticipated by “On the Formal Verification of ATM Switches”, by Jianping Lu. These rejections are traversed with respect to the presently pending claims under rejection, for at least the reasons given below.

First, it is noted that the Office Action asserts that the previously filed response failed to comply with 37 C.F.R. 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references. In reply, it is noted that the Office Action does not provide a element-by-element listing of where a particular claim element is taught or suggested in the cited art of record; rather, the Office Action merely lists each claim, and then lists portions of the cited art of record at the end of the claim. It is respectfully submitted that it is unclear which of those cited portions corresponds to which of the claim elements, and specificity is respectfully requested in the next PTO correspondence as to where a particular claim element is found in the cited art of record.

Turning now to the cited art of record, each of the presently pending independent claims (except some of the method claims that already recited certain features in an ending steps) now recite a means for determining. For example, claim 1 recites means for determining, based on the logic cones, whether logic circuits that have been designed in a behavioral synthesis phase are acceptable to be used in a manufacturing phase for the logic circuits. It appears that the Office Action did not give patentable weight to this feature, as the Office Action asserts that it was previously recited as an intended use. Clearly, this feature is now recited as a means plus function element, which must be given patentable weight.

According to the descriptions made on page 11, left column to page 12, right column of Foster, there are cases where incorrect verification can be made due to an interpretative difference between a simulator and a logic synthesis even when the technique described in Foster is used. To avoid such interpretative difference, according to Foster, it is necessary to pay attention to “coding style”. In other words, Foster describes a problem such that there are cases where incorrect verification can be made due to “simulation operation” even when the well-known technique mentioned in the Office Action is used.

In contrast, according to the present invention, correct verification can be made even when there is a simulator operation problem. According to Foster, it is necessary to pay attention to “coding style” to overcome such a simulator operation problem. Therefore, Foster is not especially pertinent to the presently claimed invention. Blackett and Lu suffer similar deficiencies.

In more detail, Foster, Blackett and Lu describe features that are similar to the prior art described on pages 5 of the specification (“JP8-22485 and Edmund Clarke et al., “Model Checking”) and pages 10 and 11 of the specification (“International Conference on Computer Design, pp. 458-466, 1999”).

In contrast, in the present invention, the object code 15 (“the object code 15 complied from the behavioral language description 12”) is obtained by a compiler compiling the behavioral level description 12 into CPU-executable form. As described on pages 11 and 12 of the specification:

This is the reason why a logic verification system is desired which can guarantee equivalence between an execution result of the object code 15

compiled from the behavioral level description 12 and an execution result of operations of the circuit obtained from behavioral synthesis.

There are also demands for formal property verification on the behavioral level description 12. In this case, since formal property verification and simulation are complimentary to each other, it is preferable that operations executed by the CPU, that is, the object code 15 can be verified.

Based on simulation results obtained by executing the object code 15 on a CPU, it can be determined whether or not the designed circuit is correct.

Accordingly, it is important that the result obtained by executing the object code 15 on the CPU is the same as the result obtained by operating the logic circuit obtained from “the RT level description 14.”

Foster, Blackett and Lu merely describe a technique for verifying “the behavioral level description 12”, and not a technique for verifying that the “object code 15” is equivalent to the RT level description 14.” Please note that “object code” is recited in each of the presently pending independent claims, whereby the use of the object code in the manner claimed in not disclosed or suggested by Foster, Blackett and Lu.

Accordingly, presently pending independent claim 1, as well as the other presently pending independent claims that recite a determining means or determining step that recite similar features (with some modifications), are not disclosed, taught or suggested by the cited art of record.

Still further, independent claim 21, which is directed to the features shown in Figure 4 of the drawings, recites “structure” that is not disclosed or suggested by the cited art of record. In particular, claim 21 recites first, second and third storage sections; first, second and third data processing devices; and a determining means. As discussed above, the Office Action does not provide an element-by-element listing of where each of these elements can be found in the cited art of record, but rather just lists portions of the cited art of record at the end of the listing of claim 21. Accordingly, it is impossible to determine which of those cited portions corresponds to which of the elements of claim 21, and in any event, a review of those cited portions does not disclose or suggest the specific structural elements recited in claim 21.

Conclusion:

Since all of the issues raised in the Office Action have been addressed in this Amendment and Reply, Applicant believes that the present application is now in condition for allowance, and an early indication of allowance is respectfully requested.

The Examiner is invited to contact the undersigned by telephone if it is felt that a telephone interview would advance the prosecution of the present application.

The Commissioner is hereby authorized to charge any additional fees which may be required regarding this application under 37 C.F.R. §§ 1.16-1.17, or credit any overpayment, to Deposit Account No. 19-0741. Should no proper payment be enclosed herewith, as by a check or credit card payment form being in the wrong amount, unsigned, post-dated, otherwise improper or informal or even entirely missing, the Commissioner is authorized to charge the unpaid amount to Deposit Account No. 19-0741. If any extensions of time are needed for timely acceptance of papers submitted herewith, Applicant hereby petitions for such extension under 37 C.F.R. §1.136 and authorizes payment of any such extensions fees to Deposit Account No. 19-0741.

Respectfully submitted,

Date July 9, 2007

FOLEY & LARDNER LLP
Customer Number: 22428
Telephone: (202) 945-6014
Facsimile: (202) 672-5399

By Phillip J. Articola

George C. Beck
Registration No. 38,072

Phillip J. Articola
Registration No. 38,819